IN THE SPECIFICATION:

Please replace the paragraph on page 12, line 20, through page 13, line 6, with the following paragraph:

A1

The difference in address setup timing between the mode of operation with address prediction enabled and the mode of operation with address prediction disabled is therefore apparent. With address prediction enabled, an earlier address valid time is provided as compared to when address prediction is disabled. That is, $T_{av, pred}$ is generally less than $T_{av, nopred}$. Note that the memory access timing (the amount of time needed for a memory address to return valid data) requirements are more stringent in non-address prediction mode than they are in address prediction enabled mode. That is, memories used in conjunction with address prediction inhibited mode should be able to return valid data faster than memories used in branch address prediction mode, since the address inputs to the memory device are valid later in the clock cycle. Alternative ~~abodiments~~ embodiments may perform a more aggressive form of address prediction in the address prediction enabled mode, and perform a less aggressive form of address ~~prediciton~~ prediction in the mode where address prediction is disabled. In this embodiment, the more aggressive form of address prediction would generally result in an earlier address valid time as compared to the less aggressive form. The less aggressive form may perform less branch prediction or substantially no branch prediction and thus result in a later address valid time. Therefore, the advantages described in reference to FIGs. 4-7 may be obtained by allowing for different levels of branch prediction rather than by simply enabling or disabling branch prediction all together.